SGS-THOMSON MICROELECTRONICS

AN1049 APPLICATION NOTE

MINIMIZE POWER LOSSES OF LIGHTLY LOADED FLYBACK CONVERTERS WITH THE L5991 PWM CONTROLLER

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The L5991 PWM controller is particularly suitable for SMPS of equipment that must comply with standards concerning energy saving. The device, optimized for flyback topology, monitors the power demanded by the load and changes the operating frequency of the converter accordingly: high frequency at heavy load, low frequency at light load.

In this way, power losses dependent on frequency are reduced at light load maintaining, at the same time, the advantages offered by a high switching frequency at heavy load.

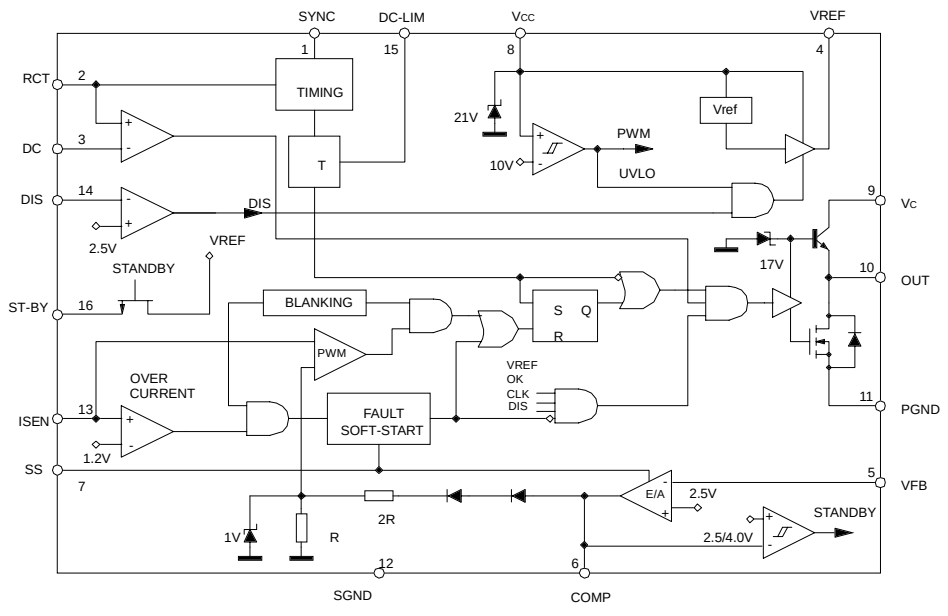
The frequency reduction is very helpful but is not the only means needed to minimize power losses. This note surveys the above mentioned functionality of the L5991 (called "Standby" function) as well as the most significant points to consider in order to achieve the goal of a very efficient lightly loaded flyback.

INTRODUCTION

The minimization of the power drawn from the mains under light load conditions (Standby, Suspend or some other idle mode) is an issue that is recently becoming of great interest, above all else because new and more severe standards are coming into force.

This is already well-established in the area of computer monitors, where norms define precisely the various idle modes and the relevant maximum consumption admitted, but more and more often power supplies for other pieces of office equipment (i.e. printers, photocopiers, fax machines, AC-DC adaptors, etc.), are required to accomplish with specifications concerning energy saving.

Figure 1. L5991 Internal Block Diagram



Anyway, minimizing the power wasted by a lightly loaded switch-mode converter is a demanding challenge for power supply designers and, to achieve the goal, an appropriate design strategy is required.

The key point of this strategy is a low switching frequency. It is well-known that many of the power loss sources in a lightly loaded flyback waste energy proportionally to the switching frequency, hence this should be reduced as much as possible. On the other hand, it is equally well-known that a low switching frequency leads to bigger and heavier magnetics and makes filtering more troublesome.

It is then desirable to make the system operate at high frequency under nominal load condition and to reduce the frequency when the system works in a low-consumption mode. This requires a special functionality of the controller: it should be able to recognize automatically the condition of light or heavy load and should adequate its operating frequency accordingly.

The L5991 PWM controller, with its "Standby function", meets exactly this requirement. The function is optimized for flyback topology: in fact, the power supply of office equipment lies most often in the medium-low power range, where flyback topology features the lowest cost/performance ratio and is, therefore, the favorite one.

However, the goal of power losses minimization cannot be achieved with only a simple reduction of the switching frequency. Although the most important, this is only one of the numerous points of a wide-ranging strategy that must be looked into on the whole.

This application note is composed of two distinct parts. The first part deals with the L5991, describes the operation of the "Standby function" in detail and states several relationships useful for the design. The second one provides an overview of the points to be considered in the above mentioned strategy, as well as a number of tips that can be helpful.

1) DESIGNING WITH THE L5991 PWM CONTROLLER

The L5991

The device, whose internal block diagram is shown in fig. 1, is based on a standard "peak" current mode PWM controller, such as the UC384x family, with the addition of numerous ancillary features among which Standby function is the most noticeable.

The L5991, which is available in DIP16 and SO16N packages, features the following characteristics:

- Very low start-up current (75 µA typ. - 150 µA max.);
- low quiescent current (7 mA typ. - 10 mA max.);
- internal reference with 1% precision guaranteed (@ Tj=25°C);
- high capability, large bandwidth, high slew-rate error amplifier;
- high-speed current loop (< 100 ns delay to output);
- high capability totem-pole output for MOSFET or IGBT drive;
- Standby function;
- IN/OUT synchronization;
- precise maximum duty cycle control;
- programmable soft-start
- 100 ns Leading Edge Blanking on current sense for increased noise immunity;
- overcurrent protection with soft-start intervention;
- latched disable function;

All these characteristics are described in detail in the datasheet of the device. In this context, however, it is worth emphasizing the low current consumption of the device, both before start-up and when running. Along with the standby function, the low consumption turns out to be particularly useful for minimizing losses. Table 1 compares these characteristics for some of the most popular devices.

Table 1 - L5991 vs. competitors

CONTROLLER	ST L5991/L5991A	Motorola MC44603	Unitrode UC3842A	Unitrode UC3823A	Linear Technology LT1242
Start-up current	75 µA typ. 150 µA max.	300 µA typ. 450 µA max.	300 µA typ. 500 µA max.	100 µA typ. 300 µA max.	170 µA typ. 250 µA max.
Quiescent current	7.0 mA typ. 10 mA max.	17 mA typ. 20 mA max.	11 mA typ. 17 mA max.	28 mA typ. 36 mA max.	7.0 mA typ. 10 mA max.
Standby function	YES	YES	NO	NO	NO

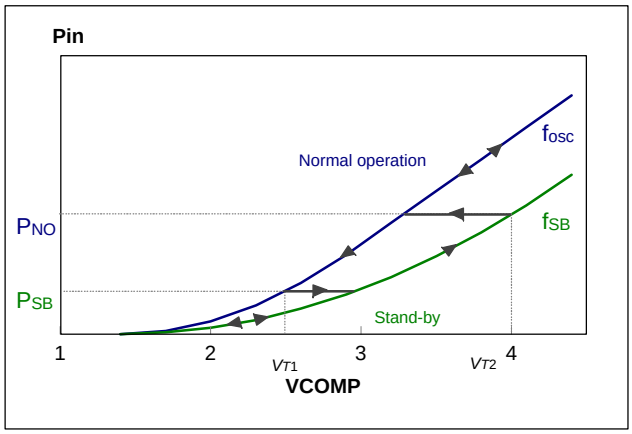
The L5991 can be used in off-line SMPS' with any single-ended topology. However, its features make the device particularly useful for power supplies based on flyback topology for office equipment that must comply with standards concerning energy saving. Monitor displays, printers, photocopiers and fax machines are the most noticeable examples.

The Standby function

The L5991 automatically detects a light load condition for the converter and decreases the oscillator frequency on that occurrence. The normal (higher) oscillation frequency is automatically resumed when the output load builds up and exceeds a defined threshold. This functionality is called "Standby function".

Like in every "peak" current mode controller, the output voltage (V_{COMP}) of the Error Amplifier (E/A) of the L5991 moves depending on the power drawn from the mains (see Appendix "Peak Current Mode Control Basics"). The basic principle of the Standby is then monitoring the E/A output .

Figure 2. Standby function dynamic operation

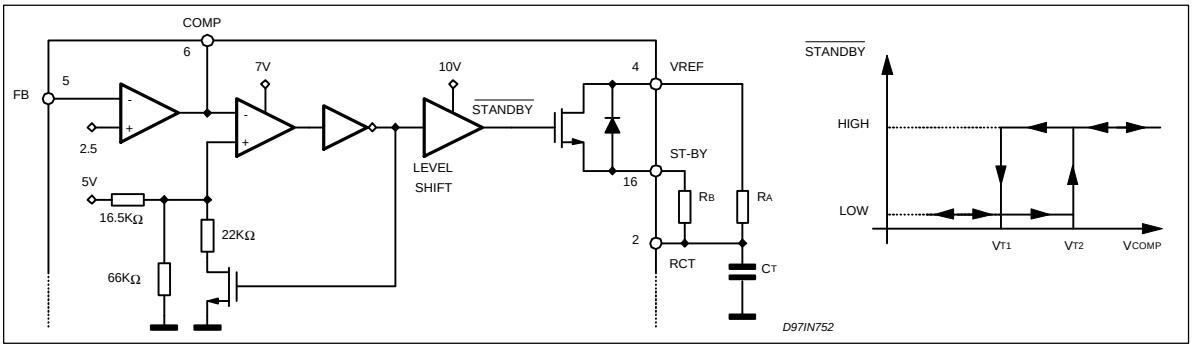


If the peak primary current decreases as a result of a decrease of the power demanded by the load V_{COMP} will decrease as well. If this falls below a fixed threshold (V_{T1}), the oscillator, which was working at f_{osc}, will be forced to work at a lower value (f_{SB}). The frequency drop, however, implies a sudden increase of the peak primary current and, therefore, of V_{COMP}. Some hysteresis will be necessary to prevent the frequency from switching back to f_{osc}. In fact, V_{COMP} will have to exceed a second threshold ($V_{T2} > V_{T1}$) in order for the oscillator frequency to be reset at f_{osc}. The hysteresis (V_{T2}-V_{T1}) will be large enough to prevent the above mentioned undesired phenomenon. This operation is shown in fig. 2.

Fig. 3 shows how the function is implemented inside the L5991. Only one pin (ST-BY, 16) is required and is used to connect externally one resistor (R_B) to the oscillator pin (RCT, 2). In this way, both the normal and the standby frequency are externally programmable.

The capacitor C_T and the resistor R_B, along with R_A, set the operating frequency of the oscillator in normal operation (f_{osc}). In fact, as long as the STANDBY signal is high, the pin is internally connected to the reference voltage VREF by a N-channel FET ($\overline{STANDBY}$; see fig. 3), thus the timing capacitor C_T is charged through R_A and R_B. When the STANDBY signal goes low the N-channel FET is turned off and the pin becomes floating. R_B is now disabled ($\overline{STANDBY}$) and C_T is charged through R_A only. In this way the oscillator frequency (f_{SB}) will be lower.

Figure 3. Standby function internal schematic and operation



The oscillation frequency can be estimated with the following approximate relationships:

$$f_{osc} \approx \frac{1}{C_T \bullet (0.693 \bullet (R_A // R_B) + K_T)} \qquad (1),$$

which gives the normal (the greater one) operating frequency, and:

$$f_{SB} \approx \frac{1}{C_T \bullet (0.693 \bullet R_A + K_T)} \qquad (2)$$

which gives the standby (the lower) operating frequency, that is the one the converter will operate at when lightly loaded. In the above expressions, $R_A // R_B$ means:

$$R_A // R_B = \frac{R_A \bullet R_B}{R_A + R_B} \qquad (3),$$

and K_T, defined as:

$$K_T = \begin{cases} 90 & V_{15} = \text{VREF} \\ 160 & V_{15} = \text{GND/OPEN} \end{cases} \qquad (4),$$

is related to the duration of the falling-edge of the sawtooth. In case V_{15} is connected to VREF, however, the switching frequency will be a half the values resulting from (1) and (2).

Fig.3 shows also the comparator with hysteresis that recognizes the load condition of the converter. The thresholds V_{T1} and V_{T2} are internally fixed at 2.5 V and 4 V respectively (typical values). The peak voltages on the current sense pin of the L5991 (ISEN, 13) relevant to V_{T1} and V_{T2} are:

$$V_{cspk1} = \frac{V_{T1} - 2 \bullet V_f}{3} = \frac{2.5 - 2 \bullet 0.7}{3} = 0.367 \text{ V} \qquad (5)$$

$$V_{cspk2} = \frac{V_{T2} - 2 \bullet V_f}{3} = \frac{4.0 - 2 \bullet 0.7}{3} = 0.867 \text{ V} \qquad (6).$$

It is more convenient to refer to the thresholds V_{cspk1} and V_{cspk2} (rather than V_{T1} and V_{T2}), because they can be immediately related to the peak input current.

Although having fixed thresholds may seem a lack of flexibility, in reality it is possible to adjust the thresholds in terms of input power level, which is just what is needed.

Standby Operation Analysis

In this context, flyback converters are classified as stated in the appendix "Flyback Basics". Another assumption is that the delay to output of the L5991 is compensated, thus the offset voltage (V_o) applied on the current sense pin is intended as the amount exceeding the value needed for compensation. This analysis does not take other non-idealities into consideration, thus the results are approximate.

Please refer to the appendix for an explanation of symbols, terminology and formulas.

When $V_{COMP} = V_{T1}$, that is on the boundary of the standby mode, the peak input current is equal to:

$$I_{ppk1} = \frac{V_{cspk1} - V_o}{R_s} = \frac{0.367 - V_o}{R_s} \qquad (7),$$

corresponding to the standby input power which, under the assumption of DCM operation, can be expressed as:

$$P_{inSB} = \frac{1}{2} \bullet L_p \bullet f_{osc} \bullet \left(\frac{0.367 - V_o}{R_s} \right)^2 \qquad (8).$$

The standby power can be expressed also in terms of the maximum input power ($P_{in\max}$). This is set by the sense resistor R_S, which is selected so as to limit the peak primary current at the value ($I_{ppk\max}$) relevant to $P_{in\max}$:

$$R_S = \frac{1 - V_o}{I_{ppk\max}} = (1 - V_o) \bullet \sqrt{\frac{L_p \bullet f_{osc}}{2 \bullet P_{in\max}}} \qquad (9).$$

By substituting (9) in (8) it is possible to obtain:

$$P_{inSB} = P_{in\max} \bullet \left(\frac{0.367 - V_o}{1 - V_o}\right)^2 \qquad (10).$$

The frequency change $f_{osc} \Rightarrow f_{SB}$ pushes flyback into a deeper DCM operation and causes a sudden increase of the peak primary current (since the input power does not change). As a result, the peak voltage on current sense will jump from V_{cspk1} to:

$$V'_{cspk1} = V_o + R_s \bullet \sqrt{\frac{2 \bullet P_{SB}}{L_p \bullet f_{SB}}} = V_o + (1 - V_o) \bullet \sqrt{\frac{P_{SB}}{P_{in\max}}} \bullet \sqrt{\frac{f_{osc}}{f_{SB}}} \qquad (11),$$

which must be $<V_{cspk2}$ not to exceed the hysteresis of the internal comparator, which would cause the operating frequency to switch back and forth between f_{osc} and f_{SB}. This constraint sets a maximum limit on the frequency change:

$$\frac{f_{osc}}{f_{SB}} < \left(\frac{0.867 - V_o}{0.367 - V_o}\right)^2 \qquad (12).$$

Provided equation (12) is fulfilled, the input power (P_{inNW}) at which the normal operation frequency is resumed ($f_{SB} \Rightarrow f_{osc}$) will be:

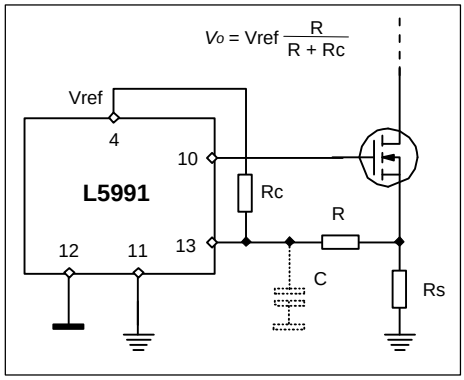
$$P_{inNW} = \frac{1}{2} \bullet L_p \bullet f_{SB} \bullet \left(\frac{0.867 - V_o}{R_s}\right)^2 \qquad (13)$$

which, considering position (9), can be also expressed in the following terms:

$$P_{inNW} = P_{in\max} \bullet \left(\frac{0.867 - V_o}{1 - V_o}\right)^2 \bullet \frac{f_{SB}}{f_{osc}} = P_{inSB} \bullet \left(\frac{0.867 - V_o}{0.367 - V_o}\right)^2 \bullet \frac{f_{SB}}{f_{osc}} \qquad (14).$$

The inspection of equations (8)...(14) shows that adding an offset V_o lowers the ratios $P_{inSB}/P_{in\max}$ and $P_{inNW} / P_{in\max}$ and raises the limit of f_{osc} / f_{SB} (with respect to the values with $V_o = 0$).

Figure 4. Circuit for the adjustment of the standby thresholds.



This is equivalent to lowering the internal thresholds V_{T1} and V_{T2}. The effect will be more pronunciated on V_{T1} than on V_{T2}. In practice, the internal thresholds have been fixed at the maximum value able to allow high enough a frequency jump, with a certain margin, leaving to an external circuit (like the one shown in fig. 4) the duty of the adjustment, if necessary.

Referring now to MCM and CCM systems, the peak voltage on the current sense pin is given by:

$$V_{cspk} = \begin{cases} V_o + R_s \bullet \left(\frac{P_{in}}{V_E} + \frac{V_E}{2 \bullet Z_E}\right) & P_{in} > P_{inT} \\ V_o + R_s \bullet \sqrt{\frac{2 \bullet P_{in}}{Z_E}} & P_{in} \le P_{inT} \end{cases} \qquad (15)$$

where Z_E is to be evaluated at $f_{sw} = f_{osc}$ or $f_{sw} = f_{SB}$, according to the operating mode. At the transition CCM $\Leftrightarrow$ DCM the peak voltage on the current sense pin will be:

$$V_{cspkT} = V_o + R_s \bullet \frac{V_E}{Z_E} \qquad (16).$$

If the sense resistor R_S is selected in the following way:

$$R_s = \frac{1 - V_o}{I_{ppk\max}} = \frac{1 - V_o}{\frac{P_{in\max}}{V_{E\min}} + \frac{V_{E\min}}{2 \bullet Z_E}} \qquad (17),$$

(with Z_E evaluated at $f_{sw} = f_{osc}$) the peak voltage on the current sense pin at transition will be given by:

$$V_{cspkT} = V_o + (1 - V_o) \bullet \frac{V_E}{V_{E\min}} \bullet \frac{2 \bullet P_{inT}}{P_{in\max} + P_{inT\min}} \qquad (18),$$

(with P_{inT} and $P_{inT\min}$ evaluated at $f_{sw} = f_{osc}$) and assumes its minimum value at minimum mains voltage (that is, @ $V_E = V_{E\min} \Rightarrow P_{inT} = P_{inT\min}$):

$$V_{cspkT\min} = V_o + (1 - V_o) \bullet \frac{2}{1 + \frac{P_{in\max}}{P_{inT\min}}} \qquad (19).$$

Table A2 in appendix shows that in MCM systems (for which $P_{inT\min} \le P_{in\max} \le P_{inT\max}$) the ratio $P_{inT\max} / P_{inT\min}$ does not exceed 3.31 in practical cases. This means that also $P_{in\max} / P_{inT\min}$ will not exceed 3.31. As a result, the transition from CCM to DCM will occur at V_{cspk} values that do not exceed 2 / (1+3.31) = 464 mV (when $V_O = 0$, and even larger values when $V_O > 0$).

In the end, since V_{cspk1} = 367 mV, when the L5991 activates the standby frequency MCM systems are operating in DCM. The standby input power will then be found once more from equation (8) which, accounting for (17) and after some manipulations, yields:

$$\frac{P_{inSB}}{P_{In\max}} = \frac{1}{4} \bullet \left(\frac{0.367 - V_o}{1 - V_o} \right)^2 \bullet \left(1 + \frac{P_{in\max}}{P_{inT\min}} \right)^2 \bullet \frac{P_{inT\min}}{P_{in\max}} \qquad (20).$$

Besides, all the considerations leading to equation (12), as well as equation (12), still apply. This will always be true if $V_{cspkT\min}$ is greater than V_{cspk1}, that is if the ratio $P_{in\max} / P_{inT\min}$ is such that:

$$\frac{P_{in\max}}{P_{inT\min}} \le \frac{1.633 - V_o}{0.367 - V_o} \qquad (21)$$

(= 4.45 for V_O =0), which includes also a class of CCM systems. In practice, the above equations apply to the large majority of common flyback designs.

Once the system is in standby mode, in equations (15) Z_E must be evaluated for $f_{sw} = f_{SB}$, becoming Z_E'. This will modify also P_{inT}, $P_{inT\min}$ and V_{cspkT}: they all increase and become $P_{inT'}$, $P_{inT\min'}$ and $V_{cspkT'}$ respectively.

When $V_{cspk} = V_{cspk2}$, that is when the input power is P_{inNW} and the frequency is to be switched back to f_{osc}, the system can be working either in DCM or CCM, depending on the f_{osc} / f_{SB} ratio and on V_E (that is, on the input voltage). In other words, it depends on whether $V_{cspkT'}$ is greater or less than V_{cspk2}. It is possible to find that if the following condition:

$$\frac{f_{osc}}{f_{SB}} \ge \frac{1}{2} \bullet \frac{0.867 - V_o}{1 - V_o} \bullet \frac{V_{E\min}}{V_E} \bullet \left(1 + \frac{P_{in\max}}{P_{inT\min}} \right) \qquad (22)$$

is fulfilled, then $V_{cspkT'} > V_{cspk2}$ and the system will be working in DCM.

The right side of (22), for V_O = 0, is top limited at 1.87 in MCM systems. Considering that in most practical cases the f_{osc} / f_{SB} ratio will not be less than 2, it is possible to leave out the case of CCM operation. This makes things easier because there would be also a dependence of P_{inNW} on V_E.

In the end, P_{inNW} will be given again by equation (13) which, rearranged more conveniently, becomes:

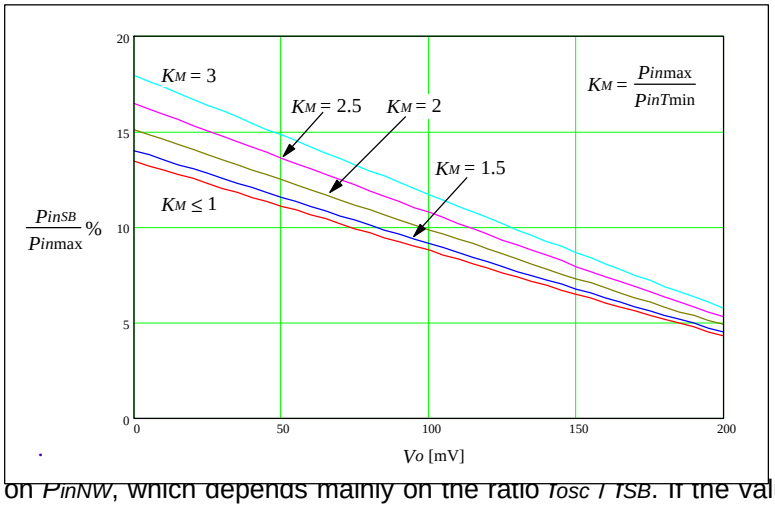
$$\frac{P_{inNW}}{P_{Inmax}} = \frac{1}{4} \bullet \left(\frac{0.867 - V_o}{1 - V_o} \right)^2 \bullet \left(1 + \frac{P_{in\max}}{P_{inT\min}} \right)^2 \bullet \frac{P_{inT\min}}{P_{in\max}} \bullet \frac{f_{SB}}{f_{osc}} \qquad (23)$$

The inspection of equations (15)...(23) shows that also in MCM systems the effect of the offset V_O is the same as in DCM systems. Furthermore, the internal thresholds V_{T1} and V_{T2} are such that a large range of applications can be covered without any external adjustment.

Standby function setup

It is difficult if not impossible to outline a general procedure for the use of the L5991's standby function because the constraints of a specific design may be of different types and are not known in advance. It is possible, however, to provide some diagrams that summarize the analysis previously carried out and that can be used for reference.

Figure 5 - P_{inSB} /P_{in}max ratio vs. DC offset on current sense



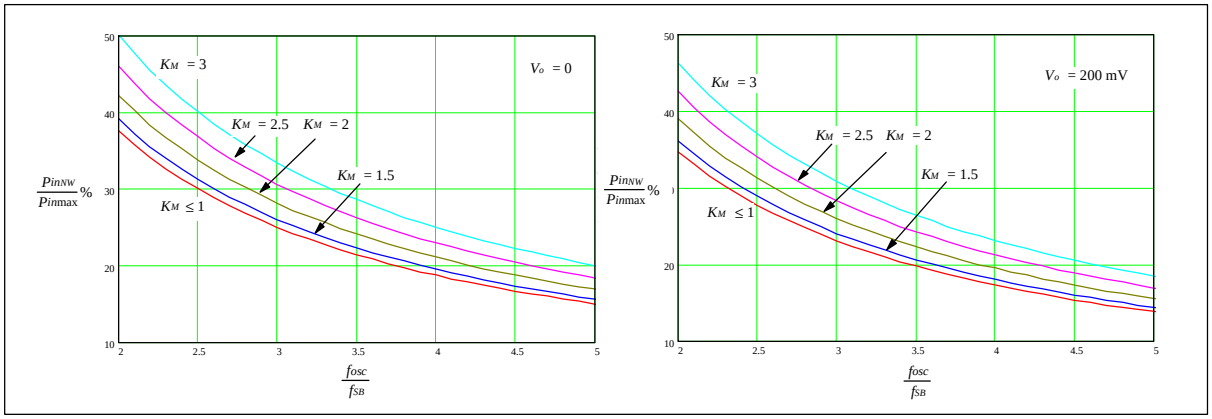
In figure 5 the ratio P_{inSB}/P_{in}max is plotted against the offset voltage on current sense V_O, for different values of the parameter K_M defined as:

$$K_M = \frac{P_{in\max}}{P_{inT\min}} \qquad (24).$$

In figure 6, the ratio P_{inNW}/P_{in}max is plotted against the ratio f_{osc} / f_{SB} for the two extreme values (0 and 200 mV) considered for V_O.

The inspection of such diagrams shows a large influence of V_O on P_{inSB}, but a much smaller influence on P_{inNW}, which depends mainly on the ratio f_{osc} / f_{SB}. If the values of f_{osc} and f_{SB} are both already fixed, there is little room for the adjustment of P_{inNW}. This is not usually a problem because there is no harmful effect if the converter is operating at f_{sw} = f_{SB} even when the load is not so light (e.g. 40% of the maximum load or even more).

Figure 6 - P_{inNW} / P_{in}max ratio vs. f_{osc} / f_{SB} ratio for 0 and 200 mV DC offset on current sense



This considering, one possible step-by-step procedure could be the following:

1. Check whether the flyback is DCM or MCM. To this end, from table (A1) pick up the value of $V_{E\min}$ relevant to the specification value and calculate $I_{ppkT\min}$:

$$I_{ppkT\min} = \frac{V_{E\min}}{Z_E} = \frac{V_{E\min}}{L_p \bullet f_{osc}}$$

   If the resulting value is greater than $1/R_s$ then the system will be DCM, otherwise MCM.
2. Calculate $P_{in\max}$. If the system is DCM use the following equation:

$$P_{in\max} = \frac{1}{2} \bullet L_p \bullet \left(\frac{1}{R_s}\right)^2 \bullet f_{osc} \qquad \text{(DCM)}$$

   otherwise use:

$$P_{in\max} = \frac{V_{E\min}}{R_s} - \frac{V_{E\min}^2}{2 \bullet L_p \bullet f_{osc}} \qquad \text{(MCM).}$$

3. Calculate $P_{inT\min}$:

$$P_{inT\min} = \frac{V_{E\min}^2}{2 \bullet L_p \bullet f_{osc}}$$

4. Calculate K_M from (24).
5. In the diagrams of fig. 5, select the curve whose K_M value is closest to the one calculated in the previous step. Then find the offset voltage V_o to be applied to the current sense pin so that the standby power P_{inSB} is close to the target value.
6. Select the curve whose K_M value is closest to the one calculated in step 4 in either diagram of fig. 6, depending on the value of V_o selected in the previous step. Then find the f_{osc}/f_{SB} ratio that better fits the target value of P_{inNW}, consistently with the constraints imposed by the specifications.
7. Calculate the new value of R_s ($R's$) needed to get the same $P_{in\max}$:

$$R_s' = R_s \bullet (1 - V_o) .$$

Standby function and error amplifier compensation

The control loop of a L5991-based flyback must be stable over a very wide range of operating conditions. These include the entire input voltage range and an input power going from P_{inSB} to $P_{in\max}$ when operating at $f_{sw} = f_{osc}$ and from $P_{in\min}$ to P_{inNW} at $f_{sw} = f_{SB}$. Moreover, the passage from standby mode to normal operation and vice versa must not have uncertainties. This requires the output of the error amplifier to react to frequency changes without overshoots and undershoots that exceed the other threshold, thus causing the oscillator frequency to switch back and forth between f_{SB} and f_{osc}.

And finally, when flyback operates in CCM, its control-to-output transfer function (dV_{out} / dV_{COMP}, where V_{COMP} is the output voltage of the error amplifier of the L5991) features the so-called RHP (Right-Half Plane) zero, which boosts the gain like a normal zero (a zero lying on the left-half plane) but lags the phase like a pole. The RHP zero, which shifts with the duty cycle, is difficult if not impossible to compensate and therefore must be kept well beyond the closed-loop bandwidth. This sometimes means that the bandwidth must be narrow.

From what told above, to achieve stability under all operating conditions, the error amplifier will need quite a heavy compensation, such that the overall bandwidth may be even narrower than $f_{SB}/4 \div f_{SB}/5$, which one could expect. As a result, the transient response of such a system will not be tremendously fast.

2) OPTIMIZING THE DESIGN FOR MAXIMUM EFFICIENCY AT LIGHT LOAD

Start-up & self-supply circuits.

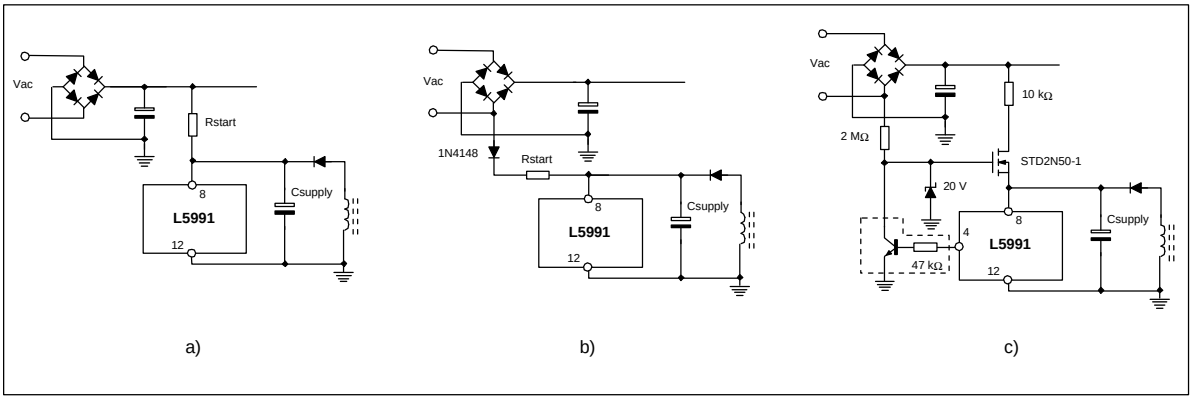
Usually the start-up circuit is most commonly realized with a resistor (*RSTART*) that draws current from the rectified and filtered DC bus (fig. 7 a). This solution is cheap but not the most efficient.

A reduction of the power dissipated at high mains voltage can be achieved by connecting the start-up resistor to the AC side of the bridge rectifier through a low-voltage diode (see fig. 7b).

In both circuits, *RSTART* carries the start-up current of the controller IC in addition to the one needed to charge the supply capacitor (*CSUPPLY*) up to the start-up threshold of the IC. This current must be ensured even at the minimum line voltage (V_{ACmin}), which imposes a limit on the maximum value of *RSTART*.

In practice, however, *RSTART* will be quite less than the maximum value, despite this increases power dissipation especially at maximum mains voltage (V_{ACmax}). In fact, the higher *RSTART* is, the less current is available to charge *CSUPPLY* and therefore the longer the supply voltage takes to reach the start-up threshold (*VTH*) of the IC, in particular at minimum mains. To reduce this wake-up time (having fixed *RSTART*), the supply capacitor should be as low as possible, accounting for the time necessary for the self-supply circuit to take over and sustain the operation of the IC (see fig. 8).

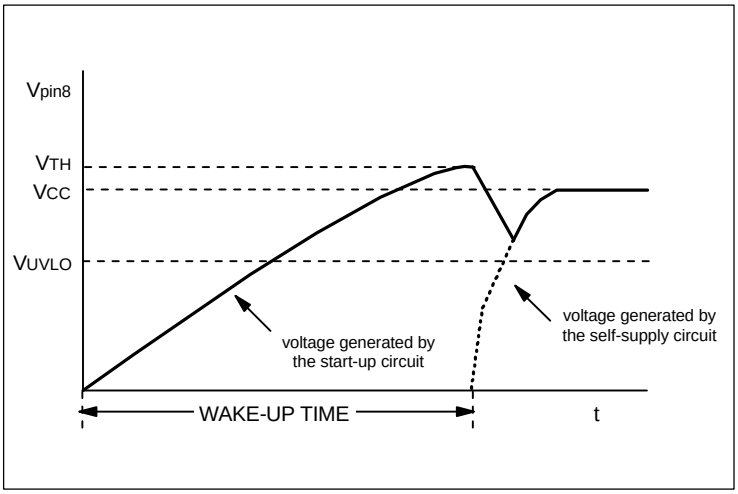
Figure 7 - Possible start-up circuit configurations



Refer to appendix "Light load losses evaluation" for the calculation of the maximum *RSTART* and an estimate of power dissipation and wake-up time.

The circuit of fig. 7c is active only during the start-up period, therefore reduces dramatically the power dissipated. Once the system is running, the start-up MOS is turned off and the only significant consumption is on the 2MΩ resistor (less than 20 mW in a wide-range mains application). The components in the dashed box can be omitted, provided the supply voltage of the IC (*VCC*) is 18 V or more, so that the gate-to-source voltage of the MOS is below the turn-on threshold.

Figure 8 - L5991 supply voltage at start-up



This circuit can deliver several mA, thus the system will wake up very quickly. On the other hand, it requires several additional parts (mainly, a small high voltage MOS) and therefore has an impact on the overall cost that needs to be evaluated by the designer.

The L5991 turns out to be very useful as to this point, compared with other controllers. Its I_{START} is low enough (150 µA max.) to achieve a reasonably low consumption even with circuits a) or b), whose main merit is to be inexpensive.

Table 2 compares the worst case consumption of the start-up circuits of fig. 7a) and 7b), at minimum and maximum mains voltage, for the devices mentioned in table 1. The table has been compiled assuming that the IC's work in a system that wakes up in 1s (@ VACmin) and where the self-supply circuit is able to keep the system operating within 10 ms, at full load. The consumption of the gate drive (see "Power MOSFET") is assumed to be 5mA and ICs' supply voltage is V_{CC} =15 V.

Table2 - Consumption of the start-up circuits of fig. 7 for different IC's

Device	C_{SUPPLY}	Start-up circuit	110 V ± 20%			220 V ± 20%			Universal Mains		
			R_{START} (kΩ)	P_{START} (mW)		R_{START}(kΩ)	P_{START} (mW)		R_{START} (kΩ)	P_{START} (mW)	
				min.	max.		min.	max.		min.	max.
L5991	33 µF	a)	200	60	150	400	140	320	200	60	640
		b)	51	60	140	120	110	270	51	60	630
MC44603	47 µF	a)	120	100	250	240	230	540	120	100	1070
		b)	33	90	220	75	180	430	33	90	980
UC3842A	47 µF	a)	110	110	270	220	250	580	110	110	1170
		b)	27	110	270	68	200	470	27	110	1190
UC3823A	82 µF	a)	75	160	390	160	340	800	75	160	
		b)	20	150	370	47	290	680	20	150	1610
LT1242	33 µF	a)	160	70	180	360	150	360	160	70	800
		b)	43	70	170	100	140	320	43	70	750

As to the self-supply circuit, usually it develops the voltage V_{CC} (obviously greater than the UVLO threshold of the IC) by rectifying and filtering the voltage generated by an auxiliary winding of the flyback transformer (see fig. 7). The power delivered by such circuit amounts at:

$$P_{SS} = (V_{CC} + V_F) \bullet (I_q + I_{GD} + I_{ext}) \qquad (25),$$

where V_F is the forward drop on the rectifier, I_q is the quiescent current of the IC, I_{GD} the average current delivered to the gate of the MOSFET by the driver output (see "Power MOSFET") and I_{ext} the current consumption of some other circuitry powered by the self-supply circuit.

It is apparent, from (25), the advantage offered by the L5991, with its 10 mA guaranteed I_q , over other controllers featuring a higher quiescent current. In addition, the Standby function reduces also the contribution due to I_{GD}.

Table 3 - Consumption of the self-supply circuit for different IC's.

Device	$I_q$max	P_{SS}max
L5991	10 mA	(15 + 0.6)V· (10 + 2)mA = 187 mW
L5991A	10 mA	(9 + 0.6)V· (10 + 2)mA = 115 mW
MC44603	20 mA	(15 + 0.6)V· (20 + 2)mA = 343 mW
UC3842A	17 mA	(15 + 0.6)V· (17 + 5)mA = 343 mW
UC3823A	36 mA	(15 + 0.6)V· (36 + 5)mA = 640 mW
LT1242	10 mA	(15 + 0.6)V· (10 + 5)mA = 234 mW

Table 3 summarizes a comparison concerning the power demanded to the self-supply circuit under light load conditions by different IC's. In addition to those considered in table 1 and 2, table 3 includes

also the L5991A, the version of L5991 with V_{TH} =9V (max.) and a minimum operating voltage of 8.2V (max.). The table assumes I_{GD} =2mA for L5991, L5991A and MC44603 (due to their standby function) and I_{GD} =5mA for the others, I_{ext} =0, V_{CC} =15V (9V for L5991A), V_F =0.6V and maximum I_q.
If the start-up circuit is (a) or (b), a low V_{CC} will cause higher power to be dissipated in R_{START}, but will also lead to a lower P_{SS}. In practical cases, the contribution of V_{CC} to P_{SS} is prevailing thus the total power consumption P_{START} + P_{SS} will be lower at low V_{CC}.

If the start-up circuit is (c) a low V_{CC} requires the use of the NPN transistor and the 47 kΩ resistor to turn off the start-up MOS, but is definitely advantageous in terms of consumption. As a result, it is advisable to keep V_{CC} as low as possible whatever start-up circuit is used.

As to this concept, the L5991A is particularly advantageous. The undervoltage lockout hysteresis, however, is small (9 - 8.2 = 0.8 V) and this calls for a bigger C_{SUPPLY} which, in turn, requires a lower R_{START} for the same wake-up time. As a result, P_{START} will be considerably higher.

The L5991A is then recommended when used in conjunction with the start-up circuit (c), or else when it is not started up directly from the mains, as considered so far (e.g. it is powered by an auxiliary power supply). In the former case the total consumption P_{START} + P_{SS} can be as low as 135 mW in an universal mains application, while in the latter only P_{SS} (≈115 mW) will be present.

Power MOSFET.

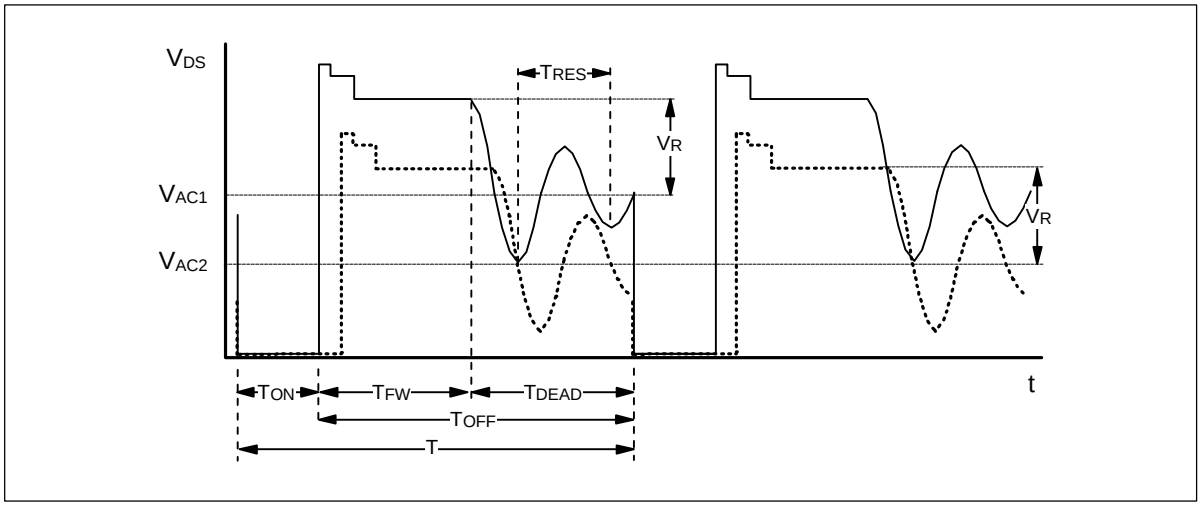
The incidence of the MOSFET on power losses at light load depends basically on the switching frequency. Leaving out conduction losses, which may be neglected in this context, the power dissipation attributable to the MOSFET under light load conditions consists of three contributions:

1 -Turn-on losses, due to the discharge of the total capacitance of the drain node inside the MOSFET. It is possible to separate two different contributions to the total drain capacitance (C_{Drain}): C_{oss}, the internal capacitance of the MOSFET, modulated by the drain voltage (manufacturers specify the value @ V_{DS}=25V), and C_{Dext}, the external parasitic capacitance due to the transformer and to the layout of the circuit. In practice, it is possible to estimate C_{Drain} from the drain voltage oscillation after the secondary current has run dry in DCM operation (see fig. 9). In fact, when the transformer is discharged, the primary inductance starts resonating with C_{Drain} and the oscillation period is:

$$T_{RES} \approx 2\pi \bullet \sqrt{L_p \bullet C_{Drain}} \qquad (26).$$

Turn-on losses depend on the input voltage in a non-monotonic way. As shown in fig. 9, the value of the drain voltage at turn-on (V_{Don}) in DCM operation is affected by the above mentioned oscillation. An input voltage increase, despite raising the settling value of the oscillation, may lead to a lower value at turn-on because of a particular combination of T_{ON}, T_{FW}, T_{DEAD} and T_{RES}.

Figure 9 - Drain voltage waveform (DCM operation)



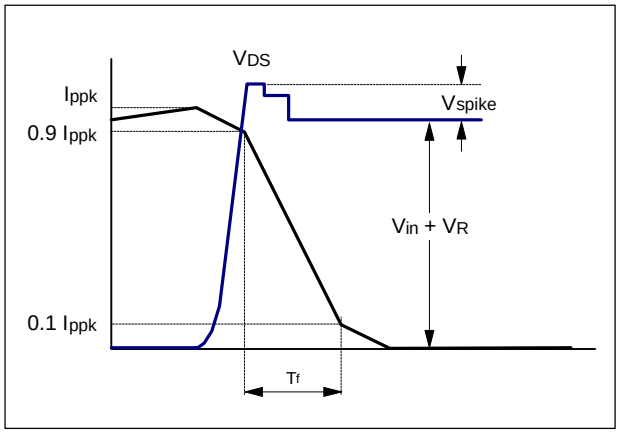
2 -Turn-off losses, due to the crossing of the active region that causes a voltage-current overlapping, as shown schematically in figure 10. The fall time (T_f) of a given MOSFET depends on the L5991 driver capability (1.6A peak) and can be controlled with a series resistor placed between pin 10 and the gate of the MOSFET.

The parasitic inductances (basically, the one located between source and ground) limit the maximum di/dt rate achievable. The rate of rise of V_{DS} depends mainly on C_{Drain}.

3 - Gate drive losses, related to the charge to be delivered to the gate each time the MOSFET is turned on. This charge, supplied at a rate given by the switching frequency, results in an equivalent DC current I_{GD}. The parameter to be considered is the total gate charge (Q_g) of the device, evaluated at the gate voltage delivered by the L5991.

Unlike the two prior contributions, gate drive losses are not wasted inside the MOSFET (except for a very small amount), but in the output stage of the L5991 and on the series gate resistor. The current I_{GD} is seen as an additional current consumption that is added to the quiescent current of the L5991 (see equation 25).

Figure 10 - Current and Voltage waveform at MOSFET turn-off



The appendix "Light load losses evaluation" helps estimate the above mentioned contributions.

When selecting the MOSFET, the parameters to look at are the voltage rating $V_{(BR)DSS}$, the on-state resistance $R_{DS(on)}$, (this only as to full load considerations), the total gate charge Q_g and the parasitic capacitances C_{iss}, C_{rss} and C_{oss}.

The $R_{DS(on)}$ should be "just what needed": low enough to reduce resistive losses at full load but not too low since Q_g, C_{iss}, C_{rss} and C_{oss} build up as $R_{DS(on)}$ decreases. It must not sound surprising to give up some efficiency points at high load in favor of an improvement at light load if that is worth it.

The voltage rating of the device should be the lowest possible. In fact, for a given $R_{DS(on)}$, the lower the $V_{(BR)DSS}$ is, the lower the total gate charge Q_g and the parasitic capacitance. A 110 V application should use a 400V device, a 220 V or wide-range application a 600 V device. The transformer plays a significant role as to this point (see "Transformer").

Last, but not least significant, the technology. A good technology device offers lower gate charge and parasitic capacitances with the same $V_{(BR)DSS}$, and $R_{DS(on)}$.

Transformer.

The design and the assembly of the flyback transformer plays a significant role in the process of power losses minimization. The most annoying parasitic is the so-called "leakage inductance", that represents the stray primary magnetic flux, modeled as an inductor in series with the primary and not coupled to the secondary. The energy stored in the leakage inductance produces an overvoltage spike on the drain of the MOSFET at turn-off. An external circuit will be necessary to clamp this spike so that the voltage rating of the MOSFET is never exceeded.

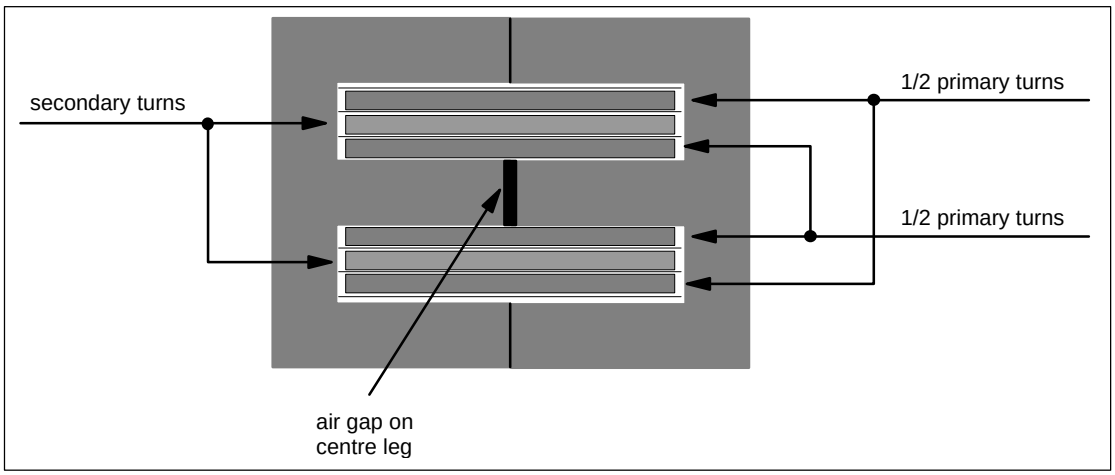
Therefore, when designing and building a transformer with the aim of optimizing the efficiency of the converter at light load, the priorities are basically three:

a) make the leakage inductance as low as possible. In terms of efficiency, there is a double noxious effect due to the leakage inductance. It not only dumps its own energy into the clamp circuit but also delays energy transfer from primary to secondary, after MOSFET turn-off, until it has run out of energy. The result is that the energy stored in the mutual inductance is not completely transferred to the secondary and is partly diverted into the clamp circuit and partly dissipated in the resistance of the primary winding. This inefficiency is worsened by a light load and a high input voltage: both reduce the primary peak current and also the voltage across the leakage inductance (the leakage inductance spike) that resets the inductance itself. The lower this voltage is, the more energy transfer is delayed and the less energy is brought to the secondary.

In practice, besides improving the energy transfer, a low leakage inductance will allow to lighten the action of the external clamp and/or to select a lower voltage rating MOSFET. This will be beneficial to efficiency at heavy load as well.

In order for a transformer to meet isolation and safety norms, primary and secondary windings must be separated by isolation layers, thus their coupling cannot be intimate. As a result, it is not possible to reduce leakage inductance below a certain extent. Practically, for a well assembled transformer, leakage inductance will be about 1÷3% of the primary inductance.

Figure 11 - Interleaved winding technique



Interleaved windings technique (putting on half the primary turns first, then all the secondaries and finally the other half of the primary; see fig. 11) can reduce leakage inductance by 50%. The two primary halves must be series connected, never paralleled.

In general, multifilar winding technique (twisting the wire of two or more windings together) gives maximum coupling between windings. In off-line converters, however, this technique is usually applicable only to secondary windings to get good cross-regulation, in case of multiple output. When multifilar winding technique is not practicable because of very different turns number (or wire size), the secondary winding with the highest output power should be wound closest to the primary; for the same power the lowest voltage should be given priority.

Other tricks, such as spacing windings evenly across a layer (when they do not completely fill it), or using multiple strands of wire, or keeping isolation between windings to a minimum are also effective to reduce leakage inductance.

Also core and coil former geometry plays an important role. To achieve good coupling, windings must be long and thin, and set out in concentric fashion. Therefore geometries with short and thick windows (such as RM, PQ or pot cores) should be avoided while ETD, EC and the majority of E cores are good. Furthermore, it is not recommended to use split coil formers, where windings are arranged side by side.

b) make the primary intrawinding capacitance as low as possible. This is the major component of the C_{Dext} capacitance earlier mentioned (see "MOSFET"). Besides contributing to MOSFET's power losses, it causes ringing and noise problems that may force the use of additional damping networks to comply with EMC requirements.

   To achieve a low capacitance, always wind first the primary winding and, in particular, the half whose end is to be connected to the drain of the MOSFET. In this way the second half primary has a shielding effect that reduces the capacitive coupling. In case of multiple layer windings, which exhibit higher capacitance, it is useful to embed one layer of isolation in between. This, however, tends to increase leakage inductance and therefore should be done with care. Split coil formers are effective to this end but, as mentioned earlier, degrade leakage inductance and then should be avoided.

c) make the reflected voltage low. As a rule of thumb, it should be below 60V in 110 V_{AC} applications and less than 100V in 220 V_{AC} or wide-range mains applications. This will reduce the voltage on the drain of the MOSFET during its OFF-time and the losses on the resistor of the clamp network

(if an RCD type is used, see "Clamp network"). Besides, a lower reflected voltage often leads to a primary-to-secondary turns ratio closer to 1:1. A positive side effect of that is a better magnetic coupling between windings, which, in turn, helps reduce leakage inductance. On the other hand, consider that a lower reflected voltage involves higher primary peak currents at heavy load.

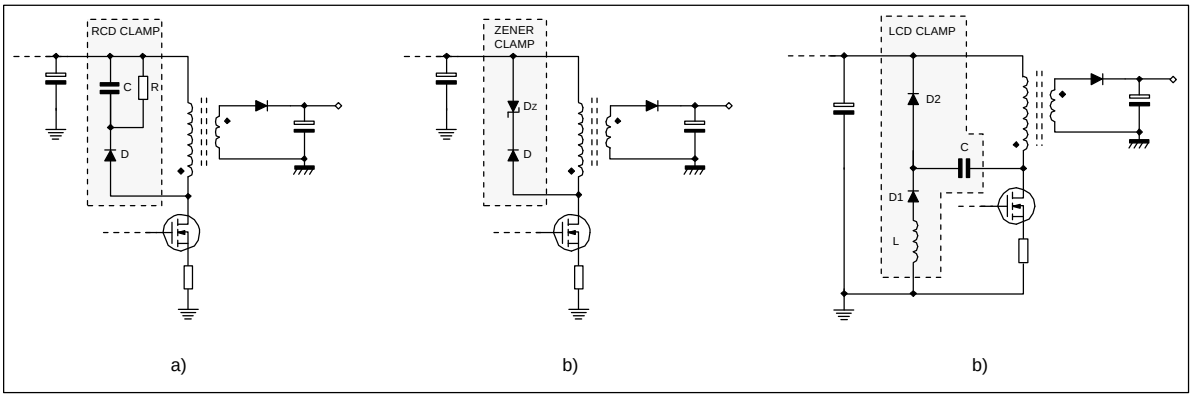
Clamp network.

Typically, the spike due to the transformer's leakage inductance is limited by an RCD clamp (see fig. 12a). Its action should be very light so as to have a spike as large as possible, consistently with the need of never exceeding the voltage rating of the MOSFET. This will optimize energy transfer from primary to secondary. A low leakage inductance of the transformer is, of course, extremely helpful.

RCD clamps dissipate power even under no-load conditions: there is always the reflected voltage across the clamp resistor (*R*). To reduce clamp losses to a negligible level at light load, the use of a zener clamp (see fig. 12b) is recommended whenever possible. Such a circuit gives also a well defined clamping level but, on the other hand, dissipates more power at full load. Its use is therefore limited to low power applications. Furthermore, a zener clamp can be more expensive than an RCD type.

An alternative to these solutions can be the use of a non-dissipative clamp like the LCD one shown in fig. 12c, which helps also reduce turn-off losses in the MOSFET. This circuit recovers the majority of the leakage inductance energy by transferring it back onto the input voltage rail. There is just a little power dissipation on the two diodes and the inductor. However, there is a slight increase of the conduction losses in the MOSFET at heavy load and, besides, the circuit is quite expensive and not easy to design.

Figure 12 - Possible clamp circuit topologies



Whatever the clamp circuit topology is, the selection of the components is not trivial but needs special care to avoid annoying problems.

The capacitors should be low-loss type (with polypropylene or polystyrene film dielectric) to reduce power dissipation and prevent overheating due to the high peak currents they experience.

The blocking diodes must be not only very fast-recovery but also very fast-turn-on type. They should be rated for repetitive peak currents greater than I_{ppk} and their voltage rating must be adequate but not much higher than necessary. For a given diode type, the higher its breakdown voltage is, the longer its turn-on time will be. This leads to higher turn-on losses and larger overvoltage spikes, extending above the clamp level, on the MOSFET's drain.

The zener diode must have an adequate power handling capability in both transient and steady state operation. The zener voltage should be approximately 50% higher than the reflected voltage so as not to have too high power dissipation at heavy load. A transient voltage suppressor (Transil) can be effectively used in place of zener diodes. Table 4 lists some recommended devices available from ST: BZV and 1N53xx types are zener diodes, all the others are Transil. SM15Txx devices are for surface mount assemblies.

Table 4 - Recommended ST's devices for clamping

	Power handling capability (steady state)				
Reflected voltage	1.7 W	2.0 W	5.0 W	6.5 W	10.0 W
$V_R \leq 50$ V	BZW04-70 BZW06-70	BZV47C68	P6KE68A 1.5KE68A	BZW50-68	SM15T68A
$V_R \leq 100$ V	BZW04-128 BZW06-128	BZV47C150	P6KE150A 1.5KE150A 1N5383B	BZW50-150	SM15T150A

Miscellaneous.

There are some other hidden losses that can be significant under light load conditions and that could be worth reducing. At least, the designer should be aware of them.

- Dummy load. Sometimes a minimum load current is required to maintain regulation and to prevent the output voltage from drifting high. A ballast resistor capable of sinking this minimum amount of current is usually placed at the output, so that the external load can be disconnected without any output voltage drift. Obviously, this resistor dissipates a constant amount of power that degrades efficiency, especially at light load, and should be removed if possible or at least minimized. The frequency reduction offered by the L5991 helps to this end.
- Feedback. The resistor divider of the feedback network (including typically an optocoupler with a voltage reference/error amplifier like the TL431) absorbs some mA, thus representing a dummy load that adds to the actual one. If possible, the feedback network should be connected to the lowest output voltage of the converter.
- Residual resistive losses. Although currents involved at light load are very low, some residual "RI^2" losses are still present. They are mainly located in the bridge rectifier, in the inrush current limiter, in the output steering diode and in the transformer, both as ohmic losses and radiation losses. Consider also that the converter is drawing very little input (real) power but much higher (up to 4-5 times) apparent power and that the RMS currents circulating upstream the input bulk capacitor are related to the apparent power.
- Case-to-heatsink parasitic capacitor. Due to the capacitive coupling of the MOSFET's package (typically, 15-20 pF for a TO220 case) to the heatsink (which is grounded for RFI reasons), current is bypassed from the drain to ground. This current does not usually generate heat but represents a dummy load. If necessary, it is possible to minimize this loss by interposing a separator, between the package and the heatsink, made up of an insulating material with a metal foil embedded in it. This halves the capacitance and therefore the current. Moreover, the foil may be a point from which a little energy can be drawn for biasing some low consumption circuit.
- RC damping networks. They are commonly used to damp ringings that generate EMI and may be located at both the primary and the secondary side. Damping is inherently dissipative, hence these RC networks should be removed. Reduction of switching speed of the MOSFET, careful PCB layout, appropriate transformer construction and selection of EMI filter components may make damping unnecessary.

Experimental results.

In order to validate the above considerations, an experimental example will be given. It concerns a 40W, wide-range mains power supply for an inkjet printer, whose design has been optimized following some of the guidelines here presented, and evaluated on the bench.

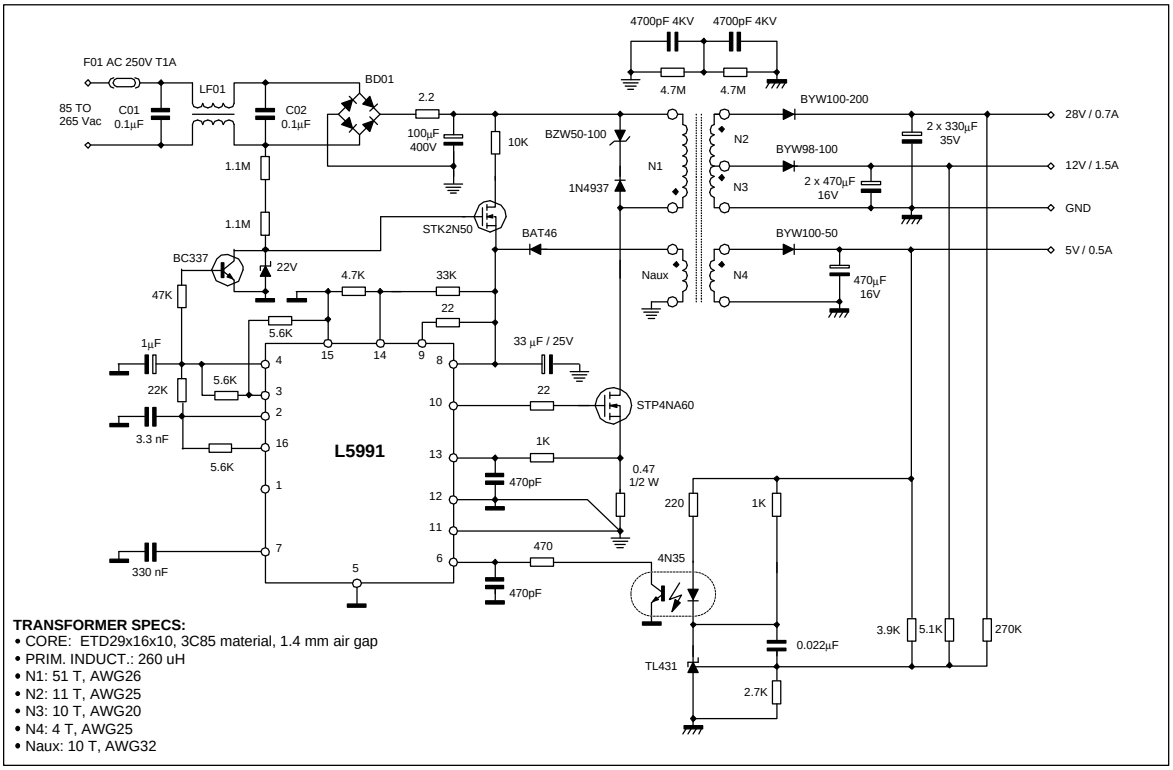
Fig. 13 shows the schematic with indication of the relevant parts. The 28V output powers the stepper motors while the 12V output supplies the printhead. When the printer is idle these two outputs are not loaded. The 5V section supplies the logic circuits as well as the µcontroller that must be operating also when the system is idle.

The system operates at 100 kHz at nominal load. This value is set by the parallel of the 22 kΩ and the 5.6 kΩ resistors connected at pin 2, along with the 3.3 nF capacitor placed between pin 2 and ground.

When the output load is decreased so that the input power falls below about 8 W, the output of the error amplifier crosses the lower threshold (V_{T1}) of the internal comparator. The L5991 now

disconnects internally the 5.6 kΩ resistor, so that the capacitor is charged through the 22 kΩ resistor only and the oscillator frequency is changed to about 20 kHz.

Figure 13 - 40W Power Supply for inkjet printers. Electrical schematic



The system works at 20 kHz as long as the input power does not exceed about 9 W. When the load current increases and this power is exceeded, the output of the error amplifier overcomes the upper threshold (V_{T2}) and the L5991 connects again the 5.6 kΩ resistor, thus switching the oscillator frequency back to 100 kHz.

The target was to draw from the line less than 2W over the entire input voltage range with the 28V and 12V outputs unloaded and with the minimum load (0.55 W) on the 5V section. The results of the evaluation are summarized in table 5.

Table 5 - 40W Power Supply for inkjet printer. Standby consumption.

Mains Voltage	85 Vac	110 Vac	160 Vac	220 Vac	265 Vac
Input Power	0.90 W	0.93 W	1.03 W	1.14 W	1.57 W
Output Power	0.55 W				

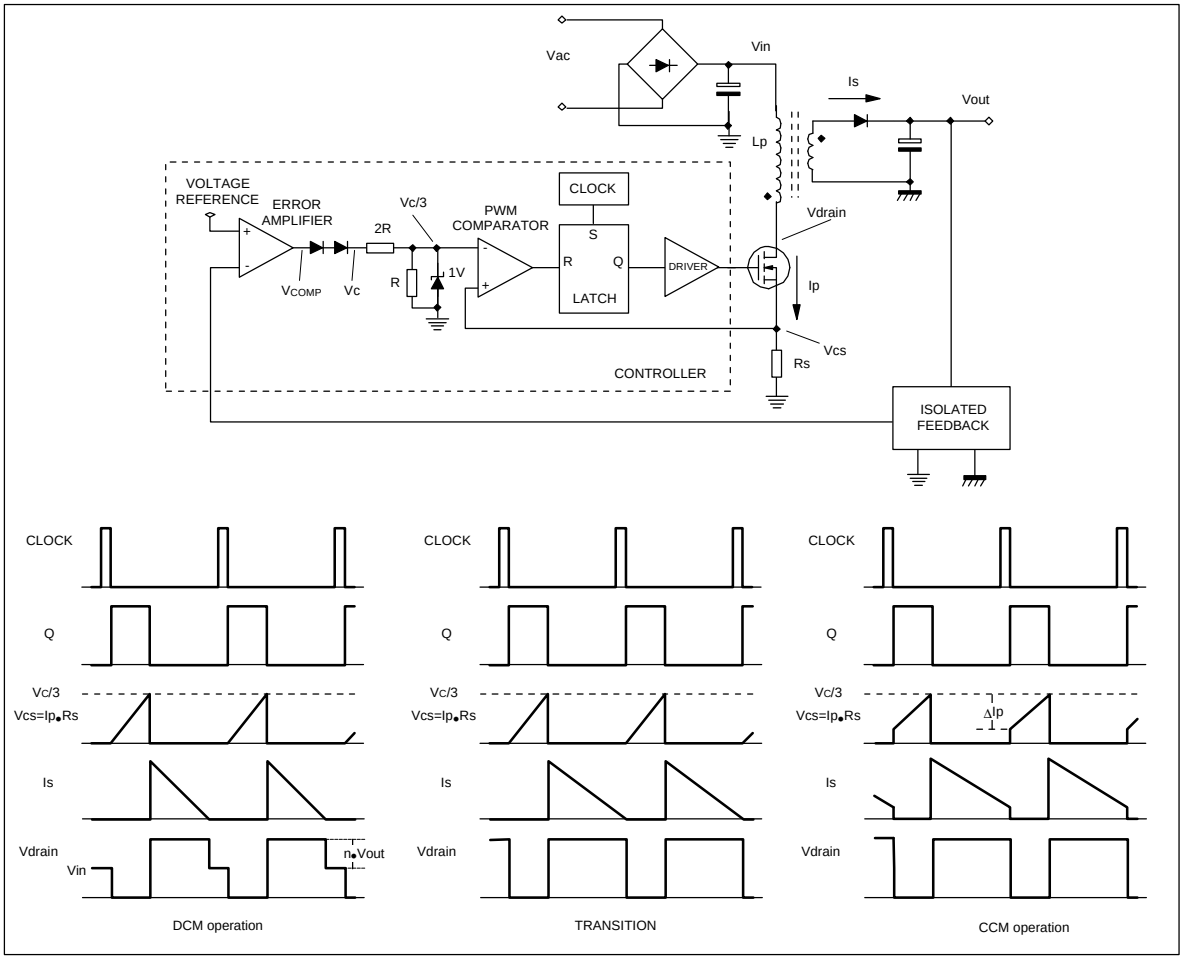
APPENDIX

Flyback Basics

Flyback's operation takes place in a two-step process. During the ON time of the switch, energy is taken from the input and stored in the primary of the flyback transformer (actually, two coupled inductors). At the secondary side, the catch diode is reverse-biased, thus the load is being supplied by the energy stored in the output bulk capacitor.

When the switch turns off, the primary circuit is open and the energy stored in the primary is transferred to the secondary by magnetic coupling. The catch diode is forward-biased, and the stored energy is delivered to the output capacitor and to the load (recirculation). The output voltage is reflected back to the primary through the turns ratio and adds up to the input voltage (typically, the filtered rectified mains), giving origin to a much higher voltage on the drain of the MOSFET.

Figure A1 - Flyback Topology with peak current mode control and associated waveforms



Flyback topology is operating in DCM (Discontinuous Current Mode) when the input -or primary - current starts from zero at the beginning of a given switching cycle. This happens because the secondary of the transformer has discharged all the energy stored in the previous period. If this energy transfer is not complete, then the primary current will start from a value greater than zero at the beginning of each cycle. Then the flyback is said to be operating in CCM (Continuous Current Mode). DCM is characterized by currents shaped in a triangular fashion, whereas CCM features trapezoidal currents (see fig. A1).

The boundary between these two types of operation depends on several parameters. Some of them are structural, that is parameters that identify the flyback converter: inductance of the primary of the transformer, transformer turns ratio and regulated output voltage. Others are related to the external world and are subject to changes: input voltage and output load. The switching frequency is usually a structural parameter, unless it is synchronized to an external signal.

As to flyback topology operating in DCM, the relationship between the peak input current (I_{ppk}) and the input power (P_{in}) is:

$$I_{ppk(DCM)} = \sqrt{\frac{2 \bullet P_{in}}{L_p \bullet f_{sw}}} \qquad \text{(A1).}$$

where L_p is the inductance of the primary of the transformer and f_{sw} the switching frequency.

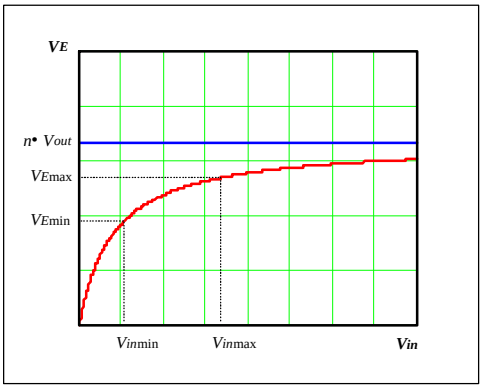
The point is: in a given flyback, when operating in DCM, the peak input current depends solely on the power drawn from the input.

The conduction time (T_{ON}, during which the MOSFET is ON) and the recirculation time (T_{FW}, during which the MOSFET is OFF and the catch diode is conducting) are respectively:

$$T_{ON} = \frac{L_p \bullet I_{ppk(DCM)}}{V_{in}} \quad ; \quad T_{FW} = \frac{L_p \bullet I_{ppk(DCM)}}{n \bullet (V_{out} + V_F)} \qquad \text{(A2)}$$

where V_{in} is the DC input voltage and n the primary-to-secondary turns ratio, V_{out} the regulated output voltage and V_F the forward drop across the catch diode.

Figure A2 - Equivalent Input Voltage vs. DC Input



The quantity $n \bullet (V_{out} + V_F)$ is the voltage reflected back to the primary during the recirculation at the secondary. In the following will be indicated with V_R:

$$V_R = n \bullet (V_{out} + V_F) \qquad \text{(A3).}$$

Under the assumption of DCM, the sum of T_{ON} and T_{FW} is less than the switching period T=1 / f_{sw}. The transition between DCM and CCM implies:

$$T_{ON} + T_{FW} = T \qquad \text{(A4)}$$

and, by combining equations (A1), (A2), (A3) in (A4), it is possible to determine the "Transition Power" (P_{inT}), that is the maximum input power at which a given flyback works in DCM (or rather the minimum input power at which it works in CCM) for a given input voltage (and a given switching frequency, if this can vary):

$$P_{inT} = \frac{1}{2 \bullet f_{sw} \bullet L_p} \bullet \left(\frac{V_{in}}{1 + \frac{V_{in}}{V_R}} \right)^2 \qquad \text{(A5);}$$

obviously, DCM will take place for $P_{in} < P_{inT}$ and CCM for $P_{in} > P_{inT}$. This equation can be rewritten as follows:

$$P_{inT} = \frac{V_E^2}{2 \bullet Z_E} \qquad \text{(A6)}$$

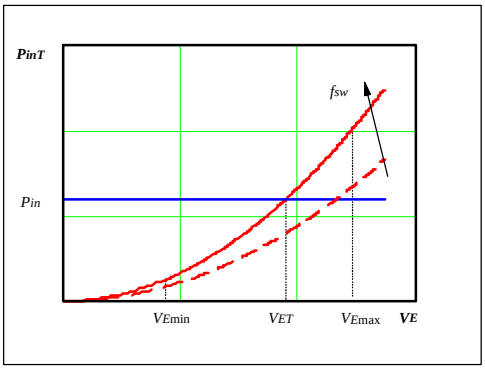
by defining the "Equivalent Input Voltage" (V_E) and the "Equivalent Primary Impedance" (Z_E):

$$V_E = \frac{V_{in}}{1 + \frac{V_{in}}{V_R}} \quad ; \; Z_E = f_{sw} \bullet L_p \qquad \text{(A7).}$$

V_E is a function of V_{in} only (see fig. A2), since the reflected voltage (V_R) is fixed. The variation of V_E in its range [V_{E}min , V_{E}max], which depends on the mains voltage range, in turn defines the range of P_{inT} [P_{inT}min ,P_{inT}max].

Fig. A3 shows the diagram of (A6) while Tab. A1 presents the ranges of V_E relevant to typical mains voltage ranges, as well as the corresponding $P_{inT}max$ / $P_{inT}min$ ratios.

Figure A3 - Characterization of the transition DCM ⇔ CCM



To complete the characterization of the transition between DCM and CCM it is convenient to define the Transition Voltage (V_{ET}), that is the Equivalent Input Voltage at which the operation is on the boundary between DCM and CCM, for a given P_{in} and a given Z_E:

$$V_{ET} = \sqrt{2 \bullet Z_E \bullet P_{in}} \qquad \text{(A8).}$$

DCM will take place for $V_E > V_{ET}$ and CCM for $V_E < V_{ET}$.

In synchronized converters it is possible to define also the Transition Frequency (f_T), that is the switching frequency at which the operation is on the boundary between DCM and CCM, for a given V_E and a given P_{in}:

$$f_T = \frac{V_E^2}{2 \bullet L_p \bullet P_{in}} \qquad \text{(A9).}$$

DCM will take place for $f_{sw} < f_T$ and CCM for $f_{sw} > f_T$.

The peak primary current at transition is then:

$$I_{ppk(T)} = \sqrt{\frac{2 \bullet P_{inT}}{f_{sw} \bullet L_p}} = \frac{1}{f_{sw} \bullet L_p} \bullet \frac{V_{in}}{1 + \frac{V_{in}}{V_R}} = \frac{V_E}{Z_E} \qquad \text{(A9).}$$

In case of CCM operation, equation (A4) still applies but the timing relationships (A2) change as follows:

$$T_{ON} = \frac{L_p \bullet \Delta I_p}{V_{in}} \quad ; \quad T_{FW} = T - T_{ON} = \frac{L_p \bullet \Delta I_p}{V_R} \qquad \text{(A10),}$$

where ΔI_p is the primary current ripple.

Table A1 - Typical V_E ranges

Mains	110 Vac ± 20%		220 /240 Vac ± 20%		Universal	
Vin	100 ÷ 175 Vdc		215 ÷ 370 Vdc		100 ÷ 400 Vdc	
	VE	***PinTmax / PinTmin***	***VE***	***PinTmax / PinTmin***	***VE***	***PinTmax / PinTmin***
VR = 50 V	33.3 ÷ 38.9	1.37	40.6 ÷ 44.0	1.18	33.3 ÷ 44.4	1.78
VR = 100 V	50.0 ÷ 63.6	1.62	68.3 ÷ 78.7	1.33	50.0 ÷ 80.0	2.56
VR = 150 V	60.0 ÷ 80.8	1.81	88.4 ÷ 106.7	1.46	60.0 ÷ 109.1	3.31

The peak primary current is no more uniquely related to P_{in} but now depends also on V_E (i.e. V_{in}):

$$I_{ppk(CCM)} = \frac{P_{in}}{V_{in}} \bullet \frac{T}{T_{ON}} + \frac{1}{2} \bullet \Delta I_p = \frac{P_{in}}{V_E} + \frac{V_E}{2 \bullet Z_E} \qquad \text{(A11).}$$

It is possible to prove that I_{ppk} is minimum when $V_E = V_{ET}$ for a given P_{in} ($>P_{inT}min$), that is at the transition, then it will be maximum for $V_E = V_{E}min$ (i.e. for $V_{in} = V_{in}min$).

It is convenient to classify flyback converters on the basis of their maximum input power $P_{in}max$:

$$P_{in\max} = \frac{P_{out\max} + P_{extra}}{\eta} \qquad \text{(A12)},$$

being $P_{out\max}$ their rated output power, P_{extra} some extra output power provided for transients or temporary overloads and η their efficiency, as follows:

- $P_{in\max} < P_{inT\min}$ ($\Rightarrow V_{ET} < V_{E\min}$): DCM flyback;
- $P_{inT\min} < P_{in\max} < P_{inT\max}$ ($\Rightarrow V_{E\min} < V_{ET} < V_{E\max}$): MCM (Mixed Conduction Mode) flyback ;
- $P_{in\max} > P_{inT\max}$ ($\Rightarrow V_{ET} > V_{E\max}$): CCM flyback.

Peak Current Mode Control Basics

The following basic relationships describing the "peak" current mode control are based on the architecture shown in fig. A1 and implemented by the L5991.

From the inspection of the schematic of fig. A1 it is possible to find the relationship between the peak primary current (I_{ppk}), the peak voltage (V_{cspk}) on the (-) input of the PWM comparator and the output voltage (V_{COMP}) of the error amplifier (E/A):

$$V_{COMP} = V_C + 2 \bullet V_f = 3 \bullet V_{cspk} + 2 \bullet V_f = 3 \bullet \left(R_s \bullet I_{ppk} + V_o \right) + 2 \bullet V_f \qquad \text{(B1)}$$

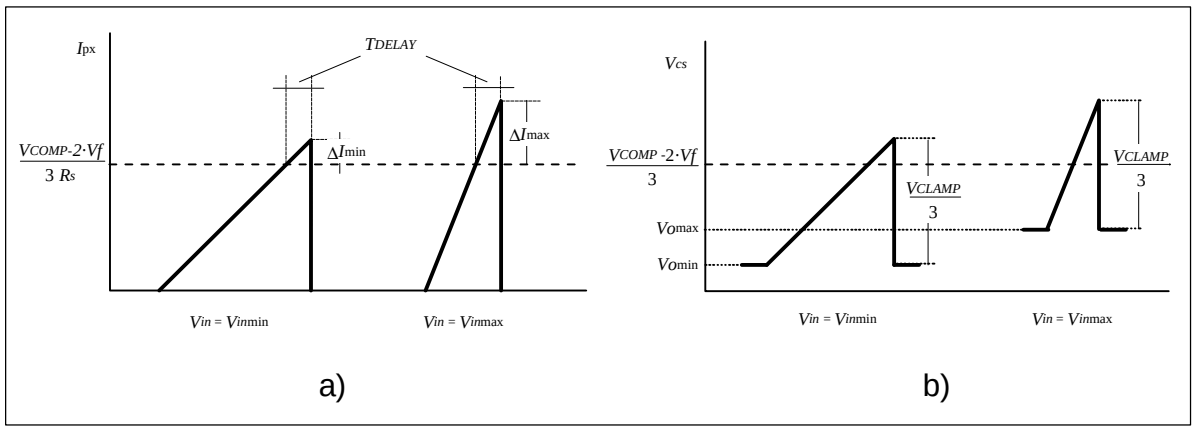
where V_f is the forward drop on each "zero duty cycle diode" (0.7V typ.) and V_o a DC offset voltage that may be applied on the (-) input of the PWM comparator (that is on the current sense pin of the L5991). V_C, the voltage downstream the two zero duty cycle diodes (and applied on the x3 divider), despite not really available, can be considered for convenience.

Considering the 1V clamp on the (+) input of the current sense comparator, V_C will be included between 0 and 3 V, and the useful swing of V_{COMP} between $2 \cdot V_f$ and $3 + 2 \cdot V_f$ volt.

Actually, equation (B1) neglects the so-called “delay to output” of the PWM controller, that is the propagation delay of the current sense path (PWM comparator + latch + driver). During this time, the switch is still ON and the input current keeps on ramping up, despite V_{cs} has already hit the internal level on (-) input of the PWM comparator.

This time lag (T_{DELAY}, 70 ns typ. 100 ns max.) is compensated by the voltage loop when the system is regulating: V_{COMP} is slightly lower than the value predicted by (B1) but the phase margin of the control loop gain gets less. Instead, when the error amplifier is saturated high and the pulse-by-pulse limiting is tripped, T_{DELAY} causes the peak current I_{ppk} to be larger than the expected limit 1 / R_s. As illustrated in fig. B1, the effect is more pronunciated as the input voltage increases.

Figure B1 - Effect of the delay to output (a) and its compensation by means of *Vo* (b)



To account for delay to output, equation (B1) should be rewritten as follows:

$$V_{COMP} = 3 \bullet \left[R_s \bullet \left(I_{ppk} - \Delta I \right) + V_o \right] + 2 \bullet V_f \qquad \text{(B2)},$$

where the current overflow ΔI is:

$$\Delta I = \frac{V_{in}}{L_p} \bullet T_{DELAY} \qquad \text{(B3).}$$

If the offset voltage is selected so that:

$$V_o = V'_o = R_s \bullet \Delta I = R_s \bullet \frac{V_{in}}{L_p} \bullet T_{DELAY} \qquad \text{(B4),}$$

the term ΔI and V_o in (B1) will annul one the other and the effect of the delay to output is eliminated.

Equation (B1) will still apply, provided V_o is regarded as the difference between the actual voltage applied on the current sense pin of the L5991 and the compensating value V'_o.

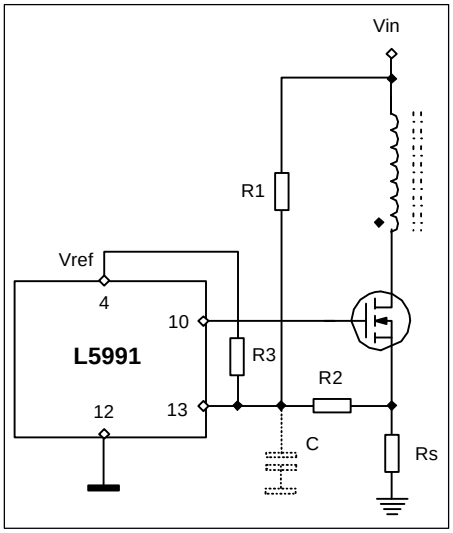
The compensation can be easily realized with the circuit shown in fig. B2. $R2$ is often used along with the capacitor C to smooth the leading edge spikes occurring when the switch turns on. In such a case only $R1$ will be added.

Considering that V'_o is in the hundred mV or less and that, therefore, $R1 >> R2$ ($R2$ is typically 1kΩ, $R1$ will be in the MΩ), perfect delay compensation will be achieved when the ratio of the two resistors is:

$$\frac{R2}{R1} = R_S \bullet \frac{T_{DELAY}}{L_p} \qquad \text{(B5).}$$

The resistor $R3$, connected to the 5V reference voltage externally available on pin 4, is used for additional offsetting the voltage on the current sense pin.

Figure B2 - Compensation of the delay to output .



Light load losses evaluation

Here follows a number of relationships useful to evaluate the major losses in a lightly loaded flyback.

Table C1 - Start-up circuits of fig. 7a and 7b

	Maximum R_{START}	P_{START}max	Maximum Wake-up time
Circuit a)	$\frac{1.41 \bullet V_{AC\min} - V_{TH}}{I_{START}}$	$\frac{(1.41 \bullet V_{AC\max} - V_{CC})^2}{R_{START}}$	$\approx C_{SUPPLY} \cdot \frac{2 \cdot V_{TH} \cdot R_{START}}{3 \cdot V_{AC\min} - V_{TH} - I_{START} \cdot R_{START}}$
Circuit b)	$\frac{0.45 \bullet V_{AC\min} - \frac{1}{2} \bullet V_{TH}}{I_{START}}$	$\frac{V_{AC\max} \bullet (V_{AC\max} - 1.35 \bullet V_{CC})}{2 \bullet R_{START}}$	$\approx C_{SUPPLY} \cdot \frac{2 \cdot V_{TH} \cdot R_{START}}{V_{AC\min} - V_{TH} - I_{START} \cdot R_{START}}$
Worst case values: V_{TH} = 16V, I_{START} = 150 µA V_{CC} is the supply voltage delivered by the self-supply circuit.			

Table C2 - MOSFET losses (refer to fig. 10)

Turn-on losses	Turn-off losses	Gate-drive current (I_{GD})	Equivalent Drain Capacitance
$\approx \frac{1}{2} \bullet C_{Drain} \bullet V_{Don}^2 \bullet f_{SB}$	$\approx \frac{I_{ppk} \cdot T_f}{2} \cdot (V_{in} + V_R + V_{spike}) \cdot f_{SB}$	$Q_g \bullet f_{SB}$	$\approx \frac{T_{RES}^2}{4\pi^2 \bullet L_p}$

Table C3 - Clamp network losses (refer to fig. 12)

RCD	Zener or Transil	LCD
$\approx \frac{V_R^2}{P}$	≈ 0	≈ 0